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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/862,471	05/23/2001	Mitsuharu Kawaguchi	NU-01007	7469

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WHITHAM, CURTIS & CHRISTOFFERSON & COOK, P.C.
11491 SUNSET HILLS ROAD
SUITE 340
RESTON, VA 20190

EXAMINER	
TREAT, WILLIAM M	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/862,471	KAWAGUCHI, MITSUHARU	
	Examiner	Art Unit	
	William M. Treat	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-12 and 16* is/are rejected.

7)☒ Claim(s) *3-4 and 13-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-4 and 6-16 are presented for examination.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 6-10 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Johnson (Superscalar Microprocessor Design).

4. The examiner has supplied pages 44-49 of Johnson which predate applicants' filing by almost a decade. They teach the concepts being claimed in claims 6-10 were old and well-known at the time of applicants' filing.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-2, 11-12, and 16 are rejected under 35 U.S.C. 103 as being unpatentable over Hunt (Patent No. 5,740,391) in view of Johnson (Superscalar Microprocessor Design).

7. Hunt taught the invention of exemplary claim 1 including an instruction buffer (316) for a pipeline processor (310) comprising: a sequence of instructions arranged in an order determined beforehand (col. 7, lines 25-67); a first buffer (342) including entries arranged in a preselected entry number order for storing said sequence of

instructions; and a second buffer (344) including other entries for storing instructions, wherein an instruction having no uncancelled dependencies and thus capable of execution stored in any one of said other entries earlier than other instructions is issued earlier than said other instructions, wherein any one instruction of said sequence of instructions stored in any one of the entries of the first buffer designated by a relatively lower entry number than another instruction in another entry is prior, in order, to another instruction stored in another entry of the first buffer different from the entry containing the one instruction designated by a relatively higher entry number than said one instruction of said sequence of instructions: and wherein said first and second buffers each issue instructions having no uncancelled dependencies and thus capable of execution in storage entry order (col. 6, lines 52-62; col. 7, lines 25-67; and Figs. 4(a-c)).

8. Applicant has added language to claim 1 detailing further their dependency based issuing of instructions and simultaneous issue of instructions from more than one buffer. Johnson taught such a method for arbitrating among instructions and issuing them from multiple buffers (pp. 46-48), and as Hunt taught: "The method of arbitrating for launching and method for launching instructions for execution may be implemented using any workable scheme" (col. 7, lines 34-43).

9. As to claim 2, Johnson taught the instruction buffer as claimed in claim 1, wherein the entries of the first buffer each show whether or not the instruction stored therein is ready to be issued. At p. 49 in the last paragraph, Johnson states: "When a result is produced, it is written to the reorder buffer and to any reservation-station entry

containing a tag for this result (this requires comparators in the reservation stations). When a value is written into the reservation stations, it may free one or more waiting instructions to be issued by providing a needed input operand." In other words, when all of an instructions operands are valid, the instruction is ready for issue from the reservation station. As to a reason for combination, see paragraph 8, *supra*.

10. As to claim 11, Hunt taught a buffer queue control for a pipeline processor comprising: a reorder buffer for registering a plurality of instructions in an order of instructions; a first buffer for storing first instructions included in the plurality of instructions; a second buffer for storing, among the plurality of instructions, second instruction other than the first instruction; said second instruction including an instruction that should be issued after said first instruction; said first buffer including a plurality of first entries for sequentially storing the first instructions in said order of instructions; said buffer queue control further comprising: means for releasing any one of the plurality of first entries that stores an instruction that issued; means for shifting any one of the first instructions that is not issued to an entry prior, in order, by one; means for issuing one of the second instructions, which can be issued, earliest in said order of instructions; and means for deleting any one of the plurality of instructions that has been executed and is earlier, in said order of instructions, than instructions not executed (col. 7, lines 34-56). Note that the pointer (PTR_EXECUTE of Figs. 4(a-c)) provides for a logical shift of instructions by one as opposed to a physical shift by one. Since applicant does not differentiate as to the type of shift, this is not a distinguishing point for applicant's claims.

11. Applicants have added language to claim 11 detailing further their dependency based issuing of instructions. Johnson taught such a method for arbitrating among instructions (pp. 46-48), and as Hunt taught: "The method of arbitrating for launching and method for launching instructions for execution may be implemented using any workable scheme" (col. 7, lines 34-43).

12. As to claim 12, Hunt taught, the buffer queue control as claimed in claim 11 further comprising the means for issuing any one of the first instructions that is earliest in said order of instructions and ready to be issued (col. 7, lines 24-56).

13. As to claim 16, if this is merely a claim for storing instructions in the buffers in program order, which inherently means in order of dependencies, and having logic circuitry to detect the resolution of dependencies before issue. Johnson taught such a method for arbitrating among instructions (pp. 48-49), and as Hunt taught: "The method of arbitrating for launching and method for launching instructions for execution may be implemented using any workable scheme" (col. 7, lines 34-43).

14. Applicant's arguments with respect to claims 1-2, 6-10, 11-12, and 16 have been considered but are moot in view of the new ground(s) of rejection.

15. Claims 3-4 and 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175.

17. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WILLIAM M. TREAT
PRIMARY EXAMINER